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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,158	10/27/2003	Michel Bardouillet	S1022.81057US00	3033
23628	7590	09/28/2004	EXAMINER	
WOLF GREENFIELD & SACKS, PC FEDERAL RESERVE PLAZA 600 ATLANTIC AVENUE BOSTON, MA 02210-2211			TRINH, HOA B	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 09/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/694,158	<b>Applicant(s)</b> BARDOUILLET ET AL.	
	<b>Examiner</b> Vikki H Trinh	<b>Art Unit</b> 2814	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-9 is/are pending in the application.  
     4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |  |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)            |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>0904</u> . | 6) <input type="checkbox"/> Other: ____  |

## DETAILED ACTION

### *Priority*

1. Acknowledgment is made of applicant's claim for priority under 35 U.S.C. 119(a)-(d) based upon an application filed in France on Oct. 31, 2001. A claim for priority under 35 U.S.C. 119(a)-(d) cannot be based on said application, since the United States application was filed more than twelve months thereafter. *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 4, and 6-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Abadeer et al. (5,418,738).

Abadeer et al. (5,418,738) discloses a resistive element controllable to irreversibly decrease its value, comprising.

As to claims 1 and 8-9, several polysilicon resistors F1a-c (fig. 3) associated in series between two input/output terminals T of the resistive element; and an assembly of switches Qfa-d (fig. 3) connected to turn the series connection into a parallel association of said resistors between two programming terminals Tb and Td (fig. 3) intended to receive a supply voltage Vdd (fig. 3). See also attachment.

As to claim 2, the switch assembly comprises one more switch Qfd than the resistive element comprises resistors F1a-c, one Td of the switches connecting one

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of said input/output terminals T to one of said programming terminals Td (fig. 3).

As to claim 4, the switch assembly comprises as many switches Qfa-d as the resistive element comprises resistors F1a-c, one of said input/output terminals being the same as one of said programming resistors. See fig. 3.

As to claim 6, each interconnection point between two resistors F1a-c (fig. 3) is connected to a first terminal of a switch Qfa-b of the assembly, the second terminal of which is connected to one of said programming terminals Tc. See also attachment.

As to claim 7, each of the resistors F1a-c (fig. 3) has identical nominal value.

### **Claim Rejections - 35 USC § 103**

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abadeer et al. (5,418,738) in view of O'Shaughnessy (5,638,029) .

Abadeer et al. (Abadeer) discloses the invention substantially as claimed. However, Abadeer does not explicitly teach that the resistive element comprises MOS transistors with N-channel transistors and P-channel transistors, whereby the number of N-channel transistors is equal to or greater than one as those p-channel transistors.

O'Shaughnessy teaches a circuit having switches, resistors, and MOS transistors with N-channel transistors (N) and P-channel transistors (P), whereby N is about equal to P or N is about one greater than P. See fig. 2.

Abadeer and O'Shaughnessy are in the same field of improving the circuit performance.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made, in view of O'Shaughnessy, to modify the invention of Abadeer with MOS transistors having N-channel transistors and P-channel transistors, whereby the n-channel transistors are equal to p-channel transistors or n-channel transistors are one greater than the p-channel transistors so as to provide a better control of the signal timing in a circuit.

### **Conclusion**

4. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Vikki Trinh whose telephone number is (571) 272-1719. The Examiner can normally be reached from Monday-Friday, 9:00 AM - 5:30 PM

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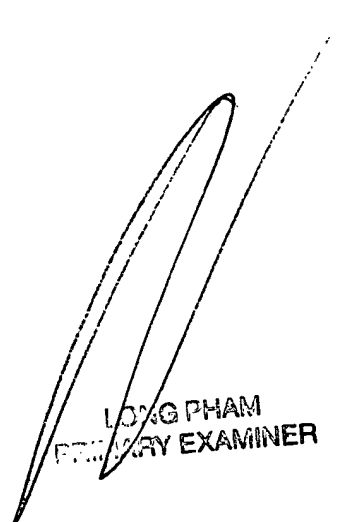
Eastern Time. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Wael Fahmy, can be reached at (571) 272-1705. The office fax number is 703-872-9306.

Any request for information regarding to the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Also, status information for published applications may be obtained from either Private PAIR or Public Pair. In addition, status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspro.gov>. If you have questions pertaining to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site ([www.uspto.gov](http://www.uspto.gov)), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at <http://www.uspto.gov/ebc/index.html> or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

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Vikki Trinh,  
Patent Examiner  
AU 2814



LONG PHAM  
PRIMARY EXAMINER



US005418738A

**United States Patent** [19][11] **Patent Number:** **5,418,738****Abadeer et al.**[45] **Date of Patent:** **May 23, 1995****[54] LOW VOLTAGE PROGRAMMABLE STORAGE ELEMENT**

[75] **Inventors:** Wagdi W. Abadeer, Jericho; Badih El-Kareh, Milton; Wayne F. Ellis, Jericho; Duane E. Galbi, Essex Jct.; Nathan R. Hiltbeitel, Essex Jct.; William R. Tonti, Essex Jct.; Josef S. Watts, South Burlington, all of Vt.

[73] **Assignee:** International Business Machines Corporation, Armonk, N.Y.

[21] **Appl. No.:** 221,515

[22] **Filed:** Apr. 1, 1994

**Related U.S. Application Data**

[62] **Division of Ser. No. 693,463, Apr. 30, 1991, Pat. No. 5,334,880.**

[51] **Int. Cl.<sup>6</sup>** ..... **G11C 17/00**

[52] **U.S. Cl.** ..... **365/100; 365/148; 365/225.7; 257/50; 257/530**

[58] **Field of Search** ..... **365/100, 148, 225.7; 257/50, 530**

**[56] References Cited****U.S. PATENT DOCUMENTS**

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E. Hamdy et al., "Dielectric Based Antifuse For Logic And Memory ICs", Transactions of the International Electron Device Meeting, pp. 786-789 (San Francisco, Dec. 1988).

**Primary Examiner**—Joseph E. Clawson, Jr.  
**Attorney, Agent, or Firm**—Sughrue, Mion, Zinn, Macpeak & Seas; Richard C. Turner; Raymond H. J. Powell, Jr.

[57]

**ABSTRACT**

A programmable storage element for redundancy-programming includes a programmable antifuse circuit, which includes a plurality of first resistors and a switching circuit for coupling the first resistors in series in response to a plurality of first control signals and for coupling the first resistors in parallel in response to a plurality of second control signals to permit programming of the first resistors, and a sensing circuit for determining whether or not the first resistors have been programmed. The state of the first resistors is determined by comparing a first voltage drop across the first resistors with a second voltage drop across a second resistor. Each of the first resistors is an unsolicited polysilicon conductor which has an irreversible resistance decrease when a predetermined threshold current is applied for a minimum period of time.

**1 Claim, 6 Drawing Sheets**